#3

FIG. 19

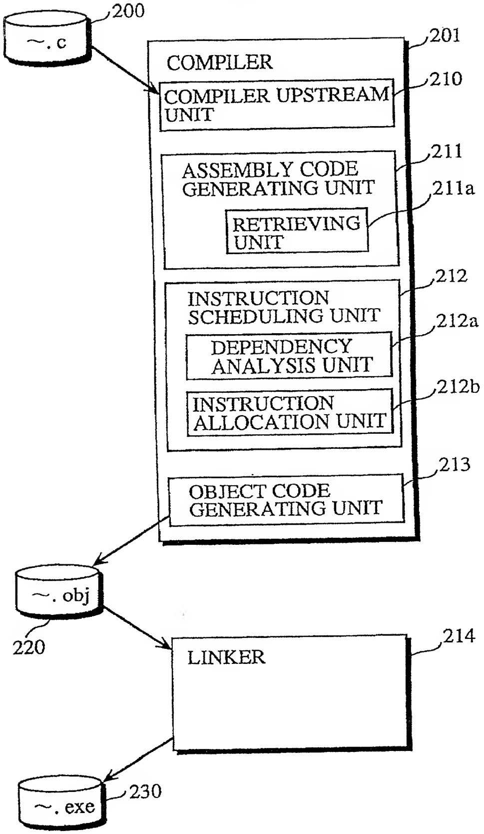

~. c
200
201
COMPILER
COMPILER UPSTREAM UNIT
210
ASSEMBLY CODE GENERATING UNIT
211
211a
RETRIEVING UNIT
INSTRUCTION SCHEDULING UNIT
212
212a
DEPENDENCY ANALYSIS UNIT
INSTRUCTION ALLOCATION UNIT
212b
OBJECT CODE GENERATING UNIT
213
~. obj
220
LINKER
214
~. exe
230

FIG. 18

LONG-WORD INSTRUCTION	FIRST INSTRUCTION SLOT	SECOND INSTRUCTION SLOT
1.	mov R1, R8	sub R2, R1
2.	mov R0, R9	sub R3, R0
3.	mov R1, R10	mul R5, R1
4.	mov R0, R11	mul R6, R0
5.	add R11, R10	add R2, R8
6.	add R3, R9	mul R7, R10
7.	add R10, R1	sub R10, R0
8.	mov R9, R12	add R8, R9
9.	sub R8, R12	mul R4, R9
10.	nop	mul R4, R12

FIG. 17

LONG-WORD INSTRUCTION	FIRST INSTRUCTION SLOT	SECOND INSTRUCTION SLOT
1.	adsb R2, R1	nop
2.	mov R1, R8	adsb R3, R0
3.	mov R0, R9	mul R5, R1
4.	add R9, R8	mul R6, R0
5.	adsb R2, R3	mul R7, R8
6.	add R8, R1	mul R4, R2
7.	sub R8, R0	mul R4, R3

FIG. 15

1. $b[0] = a[0] + a[3]$
2. $b[1] = a[1] + a[2]$
3. $b[2] = a[1] - a[2]$
4. $b[3] = a[0] - a[3]$
5. $c[0] = (b[0] + b[1]) \ast f0$
6. $c[1] = (b[0] - b[1]) \ast f0$
7. $c[2] = b[2] \ast (f1 - f2) + (b[2] + b[3]) \ast f2$
8. $c[3] = b[3] \ast (f1 + f2) - (b[2] + b[3]) \ast f2$

FIG. 16

VALUES OF PROGRAM VARIABLES
STORED IN REGISTERS

REGISTER	VARIABLE
R0	a [0]
R1	a [1]
R2	a [2]
R3	a [3]
R4	f0
R5	f1 − f2
R6	f1 + f2
R7	f2

FIG. 13

OPERATION OF CALCULATION UNIT 110

INPUT			OPERATION CONTENT
s2_op	s2_r1	s2_r2	
(1) ADD	Rn2	Rm2	STORE Rm2+Rn2 IN Rm2
(2) SUBTRACT	Rn2	Rm2	STORE Rm2−Rn2 IN Rm2
(3) ADD	Rm2	Rn2	STORE Rn2+Rm2 IN Rn2
(4) SUBTRACT	Rn1	Rm1	STORE Rm1−Rn1 IN Rm1

FIG. 14

OPERATION OF MULTIPLICATION UNIT 111

INPUT			OPERATION CONTENT
y2_op	y2_r1	y2_r2	
MULTIPLY	Rn2	Rm2	STORE Rm2∗Rn2 IN Rm2

FIG. 11

OPERATION OF DATA TRANSFER UNIT 108

INPUT			OPERATION CONTENT
X1_op	x1_r1	x1_r2	
TRANSFER	Rn1	Rm1	TRANSFER DATA FROM Rn1 TO Rm1

FIG. 12

OPERATION OF CALCULATION UNIT 109

INPUT			OPERATION CONTENT
s1_op	s1_r1	s1_r2	
(1) ADD	Rn1	Rm1	STORE Rm1 + Rn1 IN Rm1
(2) SUBTRACT	Rn1	Rm1	STORE Rm1 − Rn1 IN Rm1
(3) ADD	Rm1	Rn1	STORE Rn1 + Rm1 IN Rn1
(4) SUBTRACT	Rn2	Rm2	STORE Rm2 − Rn2 IN Rm2

FIG. 10

OPERATION OF SELECTOR 107

INPUT a2			INPUT b2			OUTPUT		
y1_op	y1_r1	y1_r2	y2_op	x2_r1	x2_r2	s2_op	s2_r1	s2_r2
(1) NO OPERATION	- -	- -	ADD	Rn2	Rm2	ADD	Rn2	Rm2
(2) NO OPERATION	- -	- -	SUBTRACT	Rn2	Rm2	SUBTRACT	Rn2	Rm2
(3) NO OPERATION	- -	- -	ADD	Rm2	Rn2	ADD	Rm2	Rn2
(4) SUBTRACT	Rn1	Rm1	MULTIPLY	Rn2	Rm2	SUBTRACT	Rn1	Rm1
(5) SUBTRACT	Rn1	Rm1	NO OPERATION	- -	- -	SUBTRACT	Rn1	Rm1
(6) NO OPERATION	- -	- -	MULTIPLY	Rn2	Rm2	MULTIPLY	Rn2	Rm2
(7) NO OPERATION	- -	- -	NO OPERATION	- -	- -	NO OPERATION	- -	- -

FIG. 9

OPERATION OF SELECTOR 106

INPUT a1			INPUT b1			OUTPUT		
x1_op	x1_r1	x1_r2	x2_op	x2_r1	x2_r2	s1_op	s1_r1	s1_r2
(1) ADD	Rn1	Rm1	NO OPERATION	- -	- -	ADD	Rn1	Rm1
(2) SUBTRACT	Rn1	Rm1	NO OPERATION	- -	- -	SUBTRACT	Rn1	Rm1
(3) ADD	Rm1	Rn1	NO OPERATION	- -	- -	ADD	Rm1	Rn1
(4) TRANSFER	Rn1	Rm1	NO OPERATION	- -	- -	TRANSFER	Rn1	Rm1
(5) TRANSFER	Rn1	Rm1	SUBTRACT	Rn2	Rm2	SUBTRACT	Rn2	Rm2
(6) NO OPERATION	- -	- -	SUBTRACT	Rn2	Rm2	SUBTRACT	Rn2	Rm2
(7) NO OPERATION	- -	- -	NO OPERATION	- -	- -	NO OPERATION	- -	- -

FIG. 8

OPERATION OF DECODER 105

INPUT	OUTPUT x2			OUTPUT y2		
	op	r1	r2	op	r1	r2
add Rn2, Rm2	NO OPERATION	- -	- -	ADD	Rn2	Rm2
sub Rn2, Rm2	NO OPERATION	- -	- -	SUBTRACT	Rn2	Rm2
adsb Rn2, Rm2	SUBTRACT	Rn2	Rm2	ADD	Rm2	Rn2
mul Rn2, Rm2	NO OPERATION	- -	- -	MULTIPLY	Rn2	Rm2
nop	NO OPERATION	- -	- -	NO OPERATION	- -	- -

FIG. 7

OPERATION OF DECODER 104

INPUT	OUTPUT x1			OUTPUT y1		
	op	r1	r2	op	r1	r2
mov Rn1, Rm1	TRANSFER	Rn1	Rm1	NO OPERATION	- -	- -
add Rn1, Rm1	ADD	Rn1	Rm1	NO OPERATION	- -	- -
sub Rn1, Rm1	SUBTRACT	Rn1	Rm1	NO OPERATION	- -	- -
adsb Rn1, Rm1	ADD	Rm1	Rn1	SUBTRACT	Rn1	Rm1
nop	NO OPERATION	- -	- -	NO OPERATION	- -	- -

FIG. 6

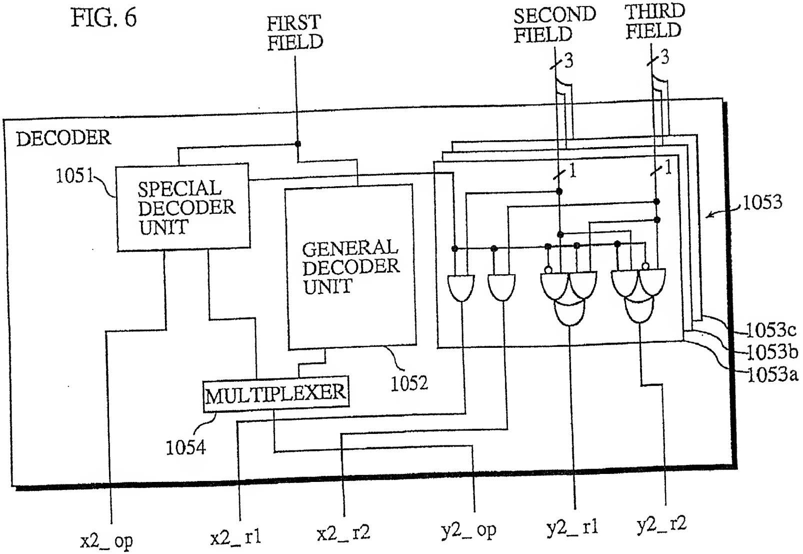

FIRST FIELD
SECOND FIELD
THIRD FIELD
3
3
1
1
DECODER
1051
SPECIAL DECODER UNIT
GENERAL DECODER UNIT
1052
MULTIPLEXER
1054
1053
1053c
1053b
1053a
x2_ op
x2_ r1
x2_ r2
y2_ op
y2_ r1
y2_ r2

FIG. 5

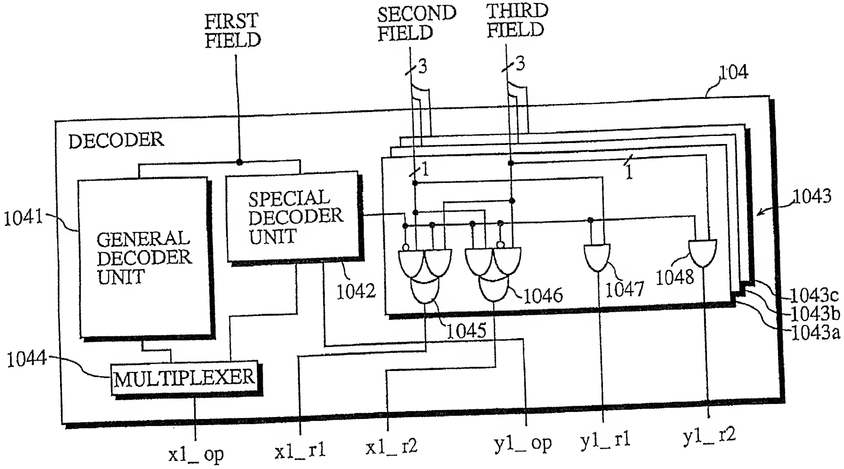

FIRST FIELD
SECOND FIELD
THIRD FIELD
3
3
104
DECODER
1
1
1043
1041
GENERAL DECODER UNIT
SPECIAL DECODER UNIT
1042
1045
1046
1047
1048
1043c
1043b
1043a
1044
MULTIPLEXER
x1_op
x1_r1
x1_r2
y1_op
y1_r1
y1_r2

FIG. 4

INSTRUCTION SETS

INSTRUCTION	MNEMONIC	PROCESSING CONTENT	ALLOCATED SLOT	
			FIRST?	SECOND?
DATA TRANSFER INSTRUCTION	mov Rn,Rm	TRANSFER DATA FROM Rn TO Rm	YES	NO
ADD INSTRUCTION	add Rn,Rm	STORE Rm+Rn IN Rm	YES	YES
SUBTRACT INSTRUCTION	sub Rn,Rm	STORE Rm−Rn IN Rm	YES	YES
ADD-SUBTRACT INSTRUCTION	adsb Rn,Rm	STORE Rm+Rn IN Rn AND Rm−Rn IN Rm	YES	YES
MULTIPLY INSTRUCTION	mul Rn,Rm	STORE Rm✱Rn IN Rm	NO	YES
NO-OPERATION INSTRUCTION	nop	NO OPERATION	YES	YES

FIG. 3

INSTRUCTION

FIRST FIELD	SECOND FIELD	THIRD FIELD
nop	0	0
mov	Rn	Rm
add	Rn	Rm
sub	Rn	Rm
adsb	Rn	Rm
mul	Rn	Rm

FIG. 2

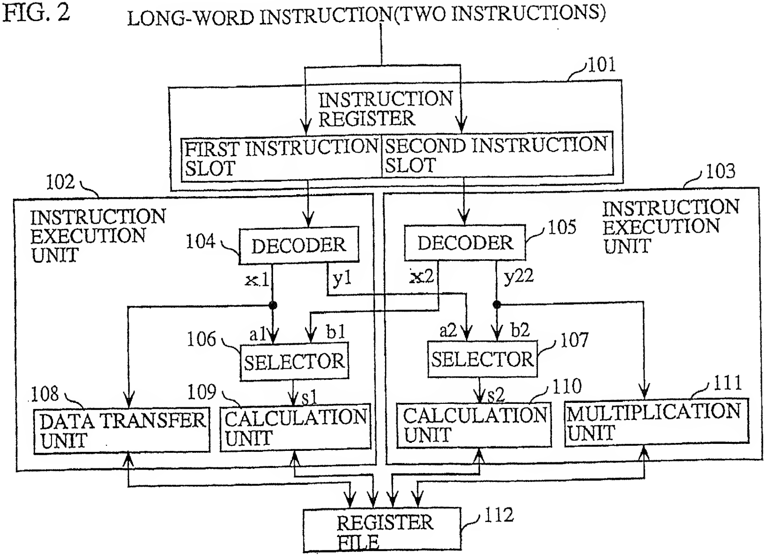
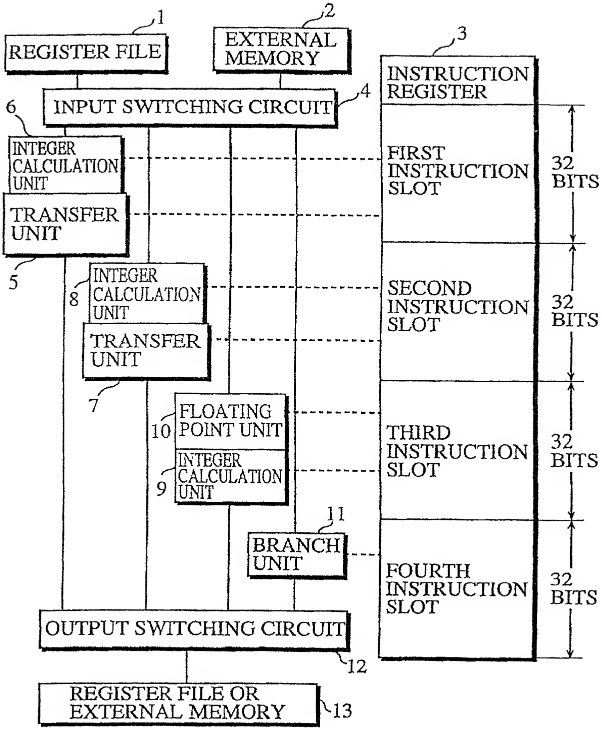

LONG-WORD INSTRUCTION(TWO INSTRUCTIONS)
101
INSTRUCTION REGISTER
FIRST INSTRUCTION SLOT
SECOND INSTRUCTION SLOT
102
INSTRUCTION EXECUTION UNIT
103
INSTRUCTION EXECUTION UNIT
104
DECODER
105
DECODER
x1
y1
x2
y22
106
a1
b1
SELECTOR
a2
b2
107
SELECTOR
108
DATA TRANSFER UNIT
109
s1
CALCULATION UNIT
s2
110
CALCULATION UNIT
111
MULTIPLICATION UNIT
REGISTER FILE
112

FIG. 1


1
REGISTER FILE
2
EXTERNAL MEMORY
3
INSTRUCTION REGISTER
4
INPUT SWITCHING CIRCUIT
6
INTEGER CALCULATION UNIT
TRANSFER UNIT
5
FIRST INSTRUCTION SLOT
32 BITS
8
INTEGER CALCULATION UNIT
TRANSFER UNIT
7
SECOND INSTRUCTION SLOT
32 BITS
10
FLOATING POINT UNIT
9
INTEGER CALCULATION UNIT
THIRD INSTRUCTION SLOT
32 BITS
11
BRANCH UNIT
FOURTH INSTRUCTION SLOT
32 BITS
OUTPUT SWITCHING CIRCUIT
12
REGISTER FILE OR EXTERNAL MEMORY
13